Process Variation and RF Performance Analysis in 10 nm FinFET Using Contact Block Reduction Method

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Outline

- 3D NEGF Self-Consistent Device Solver

- Simulation Results
  1. Comparison With Experiments
     - Source-Drain Tunneling
     - Interface-Roughness
  2. Device optimization
     - Process Variation

- Conclusions
3D NEGF Self-Consistent Device Solver (3DCBR)

- Fully self-consistent quantum mechanical transport in 2D and 3D structures (any geometry, any number of leads)
- Effective mass approximation (6 silicon valleys), different crystallographic directions
- Careful treatment of quasi-bound and pure bound states
- Electron-electron interaction (via the LDA)
- Surface/interface roughness effects
- Scattering on the local impurities
- Simple scattering on phonons (relaxation time approximation)
1. COMPARISON WITH EXPERIMENTS, SOURCE-DRAIN TUNNELING AND INTERFACE-ROUGHNESS

Transfer Characteristics

Fin extension adjustment

V_D = 0.1V

Simulation

Experiment

V_D = 1.2V

Simulation

Experiment

Drain current I_D [A/um]

Gate voltage V_G [V]

V_D = 0.1V

1E-3
1E-4
1E-5
1E-6
1E-7
1E-8
1E-9

0.0
-0.2
-0.4
-0.6
-0.8

V_D = 1.2V

1E-3
1E-4
1E-5
1E-6
1E-7
1E-8
1E-9

0.0
-0.2
-0.4
-0.6
-0.8

Gate voltage V_G [V]

Potential [eV]

Distance along the channel [nm]

Fin extension adjustment

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Subthreshold Slope

- Experiment value = 125 mV/dec
- Fin width = 12 nm
- Fin width = 10 nm
- Fin width = 8 nm
- Fin width = 6 nm
- V_D = 0.1V

Drain Current I_D [A/um]
Gate Voltage V_G [V]

Subthreshold Slope [mV/dec] vs. Fin Width [nm]
Transverse curve flattening

What do we mean?

Transfer curve flattening at low gate voltages was also observed for non-optimized FinFETs with fin thicknesses below 12 nm.

Is it Gate Leakage?

Gate leakage
**Additional Consequence of Source/Drain Tunneling**

Non-linear dependence of on-current on gate voltages is due to source-drain tunneling.

![Graph showing the relationship between drain current and source-drain voltage for different gate voltages. The graph illustrates how the drain current increases as the source-drain voltage increases, with distinct curves for different gate voltages.](image-url)
Inclusion of Interface Roughness

Exponential fit of auto-covariance of Si/SiO₂ roughness

where

\[ L_m = 8.75 \text{Å} \]

$V_D = 0.8V$

Drain current [$\mu$A/um] vs. Gate voltage [V]

Nominal

SR

% Reduction in drain current

$V_D = 0.8V$
Gate current [\mu A/\mu m]

Gate voltage [V]

\( V_D = 0.8 \text{V} \)

SR

Nominal

Gate voltage [V]

0.0 0.2 0.4 0.6 0.8

0.0 0.1 1

0.01
Cut-off frequency, \( f_{\text{cut-off}} \)

Where,
\[
g_m = \text{transconductance at } V_G = V_D = V_{\text{DD}}
\]
\[
C_g = \text{channel capacitance at } V_G = V_D = V_{\text{DD}}
\]
\[
f_{\text{cut-off}} = \frac{g_m}{2\pi C_g}
\]

Intrinsic switching speed, \( f_{\text{int_{ss}}} \)

Where,
\[
I_{\text{ON}} = \text{drive current at } V_G = V_D = V_{\text{DD}}
\]
\[
C_g = \text{channel capacitance at } V_G = V_D = 0 \text{V}
\]
\[
V_{\text{DD}} = \text{Power supply voltage}
\]

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2. Device Optimization and Process Variation

(a) Device cross-section showing Source, Gate, and Drain regions.
(b) Close-up of the Gate Oxide layer with dimensions L_g = 10 nm and t_ox = 1 nm.
(c) Vertical cross-section highlighting the Fin, Gate Oxide, and Buried Oxide layers.

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**Table:**

Desired value for different performance matrices of 10 nm DG HP devices projected by ITRS along with the simulation results obtained in this work.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>ITRS projected value</th>
<th>Simulation results</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{dd,ref}$</td>
<td>0V</td>
<td></td>
</tr>
<tr>
<td>Physical gate length [nm]</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>Electrical equivalent oxide thickness, $t_{eq}^{ox}$ [Å]</td>
<td>10</td>
<td>20</td>
</tr>
<tr>
<td>Power supply voltage [V]</td>
<td>0.8</td>
<td>0.8</td>
</tr>
<tr>
<td>Source/drain subthreshold gate-related leakage current [nA],</td>
<td>0.11</td>
<td>0.75</td>
</tr>
<tr>
<td>Effective NMOS drive current [nA],</td>
<td>2275</td>
<td>3584</td>
</tr>
<tr>
<td>Ideal NMOS device gate capacitance [nF],</td>
<td>(per gate)</td>
<td>(per gate)</td>
</tr>
<tr>
<td>Total gate capacitance for calculation of [nD],</td>
<td>(per gate)</td>
<td>$\omega \frac{C}{C_{p}}$ (per gate)</td>
</tr>
<tr>
<td>NMOSFET intrinsic delay [ps],</td>
<td>0.180</td>
<td>0.101</td>
</tr>
<tr>
<td>NMOSFET intrinsic switching speed [GHz],</td>
<td>5556</td>
<td>9901</td>
</tr>
</tbody>
</table>

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One or two channels?

\[ V_{DS} = V_{GS} = 0.8 \text{V} \]

Electron density \([\text{cm}^{-3}]\) vs. \(Z [\text{nm}]\)

- Blue line: both gates are ON
- Red line: left gate is OFF

\(t_{ox}\) and \(t_{ox}\)
Where is the centroid?

$V_{GS} = 0.8V, V_{DS} = 0V$

Electron density $[\text{cm}^{-3}]$

Potential $[\text{eV}]$
2D distribution of the change in density from off-state to on-state

\[ \Delta V_{GS} = 0.8V \]
\[ V_{DS} = 0V \]

(a) \( t_{\text{poly Si}} \)
(b) \( t_{\text{ox}} \)
(c) \( t_{\text{inv Si}} \)
Device on-current, subthreshold source-drain leakage and total gate leakage

\[ V_{DS} = V_{GS} = 0.8 \text{V} \]

\[ V_{DS} = 0.8 \text{V}, V_{GS} = 0 \text{V} \]

\[ V_{DS} = 0.8 \text{V}, V_{GS} = 0 \text{V} \]

Device on-current, subthreshold source-drain leakage and total gate leakage

\[ I_{ON} \]
**Drain current and gate current**

- For Nominal device (N):
  - $I_{ON} = 3584 \mu A/\mu m$
  - $I_{sd\_leak} = 0.75 \mu A/\mu m$

- For PS (Phonon Scattering):
  - $I_{ON} = 3360 \mu A/\mu m$
  - $I_{sd\_leak} = 1.18 \mu A/\mu m$

- For PSR (Phonon Scattering & SR):
  - $I_{ON} = 3175 \mu A/\mu m$
  - $I_{sd\_leak} = 0.67 \mu A/\mu m$

The graphs show the drain current and gate current for different conditions, with the drain-source voltage $V_{DS} = 0.8V$. The graphs compare the nominal device (N) with and without phonon scattering (PS) and with phonon scattering and SR (PSR).
2D distribution of the change in density due to a small change in gate voltage at a gate bias

1D distribution of capacitance along the channel
## Process variation: $t_{Si}$ and $t_{ox}$

<table>
<thead>
<tr>
<th>Combination</th>
<th>$t_{Si}$</th>
<th>$t_{ox}$</th>
<th>$I_{ON}$ (A/m)</th>
<th>$I_{sdleak}$ (A/m)</th>
<th>$V_{thsat}$ (mV)</th>
<th>$V_{Swing}$ (mV/V)</th>
<th>$DIBL$</th>
</tr>
</thead>
<tbody>
<tr>
<td>4 nm, 1 nm, 1 nm</td>
<td>3584</td>
<td>0.75</td>
<td>140</td>
<td>75</td>
<td>43</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4.0 nm, 1.2 nm, 1.2 nm</td>
<td>3493</td>
<td>1.15</td>
<td>130</td>
<td>80</td>
<td>55</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4.0 nm, 0.8 nm, 0.8 nm</td>
<td>3778</td>
<td>0.52</td>
<td>150</td>
<td>73</td>
<td>31</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.6 nm, 1.0 nm, 1.0 nm</td>
<td>3559</td>
<td>0.44</td>
<td>156</td>
<td>74</td>
<td>31</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.6 nm, 0.8 nm, 0.8 nm</td>
<td>3730</td>
<td>0.33</td>
<td>160</td>
<td>71</td>
<td>12</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.6 nm, 1.2 nm, 1.2 nm</td>
<td>3443</td>
<td>0.63</td>
<td>150</td>
<td>76</td>
<td>40</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4.4 nm, 1.0 nm, 1.0 nm</td>
<td>$3602 I_{ON}$</td>
<td>1.33</td>
<td>123</td>
<td>79</td>
<td>55</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4.4 nm, 0.8 nm, 0.8 nm</td>
<td>$(A/m)_{3864}$</td>
<td>0.84</td>
<td>133</td>
<td>76</td>
<td>45</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4.4 nm, 1.2 nm, 1.2 nm</td>
<td>$(A/m)_{2966}$</td>
<td>1.16</td>
<td>84</td>
<td>62</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Transfer characteristics due to fin width and gate oxide thickness variation caused by process variation

- \( V_{DS} = 0.8 \text{V} \)
- Lowest \( I_{ON} = 3443 \mu A/\mu m \)
- Highest \( I_{sd\_leak} = 2.06 \mu A/\mu m \)

- \( t_{Si} = 4.0 \text{ nm}, t_{ox} = 1.0 \text{ nm} \)
- \( t_{Si} = 4.4 \text{ nm}, t_{ox} = 1.2 \text{ nm} \)
- \( t_{Si} = 3.6 \text{ nm}, t_{ox} = 0.8 \text{ nm} \)
Values of gate leakage for all combinations due to process variation

- Gate voltage [V]
- Gate current [μA/μm]
- Gate oxide thickness [nm]
- Fin width [nm]
- Total gate leakage in μA/μm at $V_{GS}=0V, V_{DS}=0.8V$

- $t_{Si}=4.0\,nm, t_{ox}=1.0\,nm$
- $t_{Si}=4.4\,nm, t_{ox}=0.8\,nm$
- $t_{Si}=3.6\,nm, t_{ox}=1.2\,nm$

Graph shows the dependence of gate current on gate voltage for different combinations of gate oxide thickness and fin width.
CONCLUSIONS:

Quantum Transport is a MUST for modeling nanoscale devices.

Interface-roughness plays significant role in determining the switching speed of the nano-transistors.

Near optimal device can be found that performs very close to ITRS requirements.

Process variations must be taken into account in circuit designs.