Directions for simulation of beyond-CMOS devices

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Outline

Challenges and responses in nanoelectronic simulation
Limits for electronic devices and motivation for non-charge-based computing
Simulations of spintronic devices
Nonequilibrium spin devices and power dissipation
New architectures – QCA etc.
Transistor Nanotechnology

Beyond CMOS, in this talk

- Spin Molecular Optical Phase
- Other ?????

Source: Intel

Future options subject to change
The phonon-limited mobility is degraded in narrow wires over the planar MOSFET mobility. R. Kotlyar et al., Appl. Phys. Lett. 84, 5270 (2004), Intel.
Carbon nanotubes and carbon nanoribbons

Mobility increases with size
CNR have better mobility for the same size
CNT have better mobility for the same bandgap
Nanoelectronic simulations

Challenge: find the best option for the nanoelectronic transistor

Response: Industry is far along in simulation of the ultimate CMOS. Nanowire, carbon nanotube, and carbon nanoribbon transistors have been looked at. None was found to have a decisive advantage vs. CMOS.

Directions:
- predict a nanoelectronic device dramatically better than CMOS
- prove when quantum transport simulation necessary (i.e. drift-diffusion-Schrodinger-Poisson breaks down)
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Quantum limit of MOSFET

Size limited by quantum confinement
Switching time determined by the time-energy uncertainty relation
Energy set by the barrier height $\sim kT$; margin against thermal noise.

MOSFET is optimal electronic switch

Current CMOS device scaling towards the ideal limit

* Data courtesy of Robert Chau (Intel)
**Additional technology entries**

**Electric charge**
- FET, 1D structures, RTD, SET

**Electric dipole**
- ferroelectric, QCA

**Magnetic dipole/spin**
- spintronics, magnetic QCA, nanomagnetics

**Light intensity**
- photonics

**Mechanical position**
- nano-electro-mechanical systems (NEMS)

**Orbital state**
- metal-insulator, order-disorder, ion or molecular orbit

**Quantum state**
- quantum interference, RSFQ (superconducting, entanglement “quantum computing”)
Energy vs. Length

Spintronics achieves a lower power dissipation limit.
NEMS and photonics are too power hungry.
Computing limits and non-charge based logics

Challenge: choose best non-charge-based device

Response: All electronic devices obey the limit arising from fundamental physics. Need to explore non-charge-based devices to continue scaling. Many risky and immature alternative logics. No clear advantage vs. CMOS.

Directions:
- tools for simple simulation of non-charge-based devices
- predict which options are dramatically better than electronics
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Quantum transport through tunneling barrier

Nonequilibrium Green’s functions for transport.
Split spin bands in ferromagnets.
Neglect charge density - linear potential (for now).
Obtain tunneling magnetoresistance.

Intel (unpublished).
Similar to approach of Yanik, Klimeck, and Datta, Purdue U., cond-mat/0605037
DOS and occupation \( \text{Vsd}=0.6\text{V} \) anti-parallel

Plots - electron density, density of states, spin polarization. White line – top of the barrier
Current and spin current $V_{sd}=0.6V$ anti-parallel

The P and AP cases differ by a subtle balance of the positive and negative parts of current spectrum.
Tunneling magnetoresistance

Predicts decrease of TMR vs. voltage, Intel (unpublished)
Predicts inverse magnetoresistance !!! which is observed experimentally.
Simulation of spintronic devices

Challenge: simulation capability to enable experimental demonstration of a practical spintronic device


Directions:

- general spintronic simulator, handling most of proposed devices
- achieve predictive power by close interaction with experimentalists
- to filter device options, not to discover new phenomena
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Momentum and spin relaxation

in bulk GaAs
Dyakonov-Perel and
Elliott-Yafet mechanisms

Spin relaxation is slower than momentum relaxation.
easier to isolate spin from the environment, out of equilibrium.

<table>
<thead>
<tr>
<th>Material / system</th>
<th>equilibration time</th>
<th>Length scale</th>
<th>Comments</th>
<th>Reference</th>
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<tr>
<td>Bulk silicon @ 300K</td>
<td>$1 \times 10^{-13}$ sec</td>
<td>electron equilibration time</td>
<td>E.Pop et.al Journal of HeatTransfer, Vol 128, July 2006</td>
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<td>Bulk silicon @ 300K</td>
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<td>Bulk silicon @ 300K</td>
<td>$8 \times 51 \times 10^{-12}$ sec</td>
<td>41nm - 260 nm</td>
<td>Acoustic phonons</td>
<td>A Balandin CNSI – FENA Seminar, UCLA February 22, 2005</td>
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<td>Bulk silicon @ 300K</td>
<td>$7.6 \times 10^{-14}$ sec</td>
<td>7.6 nm</td>
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<td>Si 28 lattice at 300K</td>
<td>$1 \times 10^{-3}$ sec</td>
<td>electron bound to defect</td>
<td>T.D. Ladd, et.al, PHYSICAL REVIEW B 71, 014401 (2005)</td>
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<tr>
<td>Si 28 lattice at 300K</td>
<td>$1.5 \times 10^{3}$ sec</td>
<td>Nuclear spin</td>
<td>T.D. Ladd, et.al, PHYSICAL REVIEW B 71, 014401 (2005)</td>
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<tr>
<td>Diamond films at 300K</td>
<td>$1.5 \times 10^{3}$ sec</td>
<td>15 nm</td>
<td>Nitrogen - vacancy pair</td>
<td>Gaebel et. al, Nature Physics, Vol 2, June 2005</td>
</tr>
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</table>
Stages of computation

Clock field aligns spins gives them

Set the initial value +z or -z

Switch the state from +z to -z

Apply field to induce state splitting to measure spin (magnetic STM)*

Spin magnitude decreased - time for another clocking

No energy barrier between the computational states!

*Spin state destroyed by reading. Not used till next clock cycle. Only few spins are read.
Clocking is the main source of dissipation

\[ s_c = \frac{\hbar}{2} \tanh\left( \frac{\hbar GB_c}{2k_B T} \right) \hat{x} \]

need to stop after this time and refresh the magnitude of spin

\[ \tau_c = 0.1 / \gamma I (\Omega_0) \approx 33 \text{ns} \]

Energy dissipated as spin aligns to clocking field

\[ \Delta E_{tot} = k_B T \tanh(1) \frac{\tau_{sw}}{\tau_c} \]
\[ = 4.8 \cdot 10^{-5} k_B T \]

Nonequilibrium computing

Challenge: can one lower power dissipation via operation out of thermal equilibrium?

Response: Lower power dissipation is predicted in a simple spin model.

Directions:
- practical device scheme
- prove advantage vs. electronic logic
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Quantum cellular automata logic gates

- **A=1**
  - B=1
  - C=0
  - Out=1

- **NOT**
  - A=1
  - Out=0

- **MAJORITY**

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<th>C</th>
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- **AND**

- **OR**

States in cell oriented along the preferred axis, e.g. easy axis of a magnet.
Magnetization in LSMO on STO

Example of inverter and a majority gate. Operation determined by the material, shape and stress anisotropy. Intel (unpublished)
Non-traditional architectures

Challenge: what are the architectures of choice for beyond CMOS devices

Response: QCA architecture is one example specifically suited for spintronics.

Directions:
- simulator with device-circuit link for beyond CMOS devices
- which architecture brings out the best performance of non-charge-based devices
- any application-specific architecture for beyond CMOS that is dramatically better than CMOS

The (computer) clock is ticking !!!
BACKUP SLIDES
Mass and bandgap

Trend: bandgap proportional to mass. Similar values in semicon., carbon nanotubes, nanoribbons.

7.5nm 0.4nm carbon nanotube diameter
11nm 0.6nm graphene nanoribbon width
Which material is best for on-current?

\[
\Delta V = 0.7V
\]
\[
t_{ox} = \text{var}
\]
\[
\epsilon = 16
\]
\[
L = 10nm
\]

Optimal material depends on device parameters.
<3x variation of drive current.

7.5nm 11nm

0.4nm carbon nanotube diameter
0.6nm graphene nanoribbon width
Requirements to logic devices

**Performance (esp. speed)**
Architectural compatibility w CMOS (connections, voltage range)

Stability and reliability
CMOS process compatibility (fabricated on the same wafer)
Room temperature operation

**Energy efficiency (energy per switching)**
Low sensitivity to parameters (e.g. fabrication variations)

**Scalability (remains functional as size shrinks)**

* After ITRS 2003
### Evaluation of Alternative Logic

**Table 67  Technology Performance and Risk Evaluation for Emerging Research Logic Device Technologies (Potential/Risk)**

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<td>SETs</td>
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<td>QCA Devices</td>
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<td>1.6/1.1</td>
<td>2.0/1.4</td>
</tr>
</tbody>
</table>

Two numbers:
- Performance potential
  - 3 = better than CMOS
  - 2 = comparable to CMOS
  - 1 = worse than CMOS
- Risk
  - 3 = solutions known
  - 2 = concept feasible
  - 1 = no known solution

International Technology Roadmap for Semiconductors 2004
http://www.itrs.net/Common/2004Update
Correlated metal oxides

Materials like LaSrMnO$_3$ exhibit Ferroelectric, ferromagnetic, antiferromagnetic, metal, insulator regions depending on stoichiometry.